

these amendments be entered under the provisions of 37 C.F.R. § 1.116(b) for the purposes of placing the application in condition for allowance or for the purposes of appeal.

Attached hereto is a marked-up version of the changes made to specification and claim 9 by the current amendment. The attached pages are captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

The Official action approved the changes to the drawings, which were proposed in the request for approval of drawing changes filed on December 13, 2001. Accordingly, applicant is filing together herewith a transmittal of drawings including corrected Figs. 6 and 7.

Claims 1-9 remain in the application for consideration by the examiner. These claims were discussed in a personal interview with Examiners Chris C. Chu and Eddie Lee on May 14, 2002. Applicant desires to express thanks to the examiners for the courtesies extended the undersigned. At the interview, the case of *In re Rose*, which was cited in the outstanding Office Action, was discussed. The undersigned explained that this case is not very pertinent to the presently claimed invention. In particular, the numerical limitations in applicant's claims are not directed to a change in size, but rather, are directed to structure that has advantages not contemplated or suggested by the teachings cited thereagainst. After some discussion, the examiners suggested that the applicant submit a response explaining the importance and significance of the numerical limitations in the claims. The importance and

significance of the numerical limitations in the claims is discussed in detail below.

The Official action set forth three different prior art rejections of the claims. The first two were rejections of Claim 1 under 35 U.S.C. § 103(a) as being unpatentable over either U.S. Patent No. 4,418, 467 of Iwai or U.S. Patent No. 6,268,641 of Yano. The third rejection was a rejection of Claims 2-9 under 35 U.S.C. § 103(a) over Yano in further view of U.S. Patent No. 6,004,405 of Oishi *et al.* (Oishi). These same three teachings were cited against applicant's claims in the previous Office action. In all these rejections, it was acknowledged that the teachings of the cited references do not teach a dot mark having a maximum length of 1 to 13 μm on an inner wall surface of a notch formed on an outer peripheral face of the semiconductor wafer. However, the position was taken that it would have been an obvious matter of design choice to change the dot mark to have a maximum length of 1 to 13 microns on an inner face wall of a notch formed on an outer peripheral face of the semiconductor wafer, because such a modification would have involved a mere change in the size of a component. The Official action stated that change in size is generally recognized as being within the level of skill in the art, citing *in re Rose*, 105 USPQ 237 (CCPA 1955).

Applicant respectfully submits that the teachings of Iwai, Jeng, Yano and/or Oishi either taken alone or in combination do not contemplate or

suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103.

The prior art rejections set forth in the Official action are mainly based on the issue: that changing the dot mark to have a maximum length of 1 to 13 microns on an inner face wall of a notch formed on an outer peripheral face of a semiconductor wafer would have been obvious, because such a modification would have involved a mere change in the size of a component. In the presently claimed invention, the size of the dot marks of a maximum length of 1 to 13 μm , and the location of the marks on an inner face wall of a notch formed on a outer peripheral of the face of the semiconductor wafer, enable the marking of individual semiconductor wafers for the purposes of identifying the wafers. The prior art was unable to mark the wafers individually and generally relied upon batch numbering. Thus, applicant's invention provides a manner of identifying each individual semiconductor wafer, which is important for providing superior quality of the semiconductor wafers. The teachings of Iwai, Jeng, Yano and/or Oishi do not remotely contemplate or suggest the structure or resulting function of applicant's claims.

For the examiner's review, applicant is attaching hereto the front and back covers of IEEE transactions on Semiconductor Manufacturing Special Section on the 2000 International Synopsis on Semiconductor Manufacturing (ISSM 2000) and subsequent pages 177-186. Within these pages, pages 180-186 are a paper entitled "New Microcharacters for Wafer Identification." This is

one of four papers that were selected based on the scoring of recommendations by the members of ISSM 2000 Program Committee (see page 178, last paragraph and left column, "Guest Editorial Special Section on ISSM 2000"). This means that those persons skilled in this art recognized that the paper entitled New Microcharacters for Wafer Identification was important and significant in this art. One of the authors of this paper, Teiishrou Chiva, is one of the inventors of the present application.

Fig. 1 of the paper the paper entitled New Microcharacters for Wafer Identification shows the microlocation of conventional ID on the surface of the semiconductor wafer. This figure also shows the new micro ID in a V-shaped notch in accordance with applicant's claims. Figures 13(a) and 14(a) of the paper show reading images for new microcharacters in the V-shaped notch, and Figs. 13(b) and 14(b) show reading images for conventional characters on the surface. In Figs. 13(a) and 14(a), it can be seen that the sizes of the dot marks are in the range of 1 to 13 microns, in accordance with the presently claimed invention. The advantageous effect of the microcharacter ID system (which is set forth in applicant's claims) is described, for example, in a portion of the paper under the subtitle "B. Comparison with Conventional IDs" on page 184. In particular, the second paragraph of this portion reads that:

..., considering the marking location, the microcharacter enable marking ... in a V-shaped notch on a wafer. As a result, the influence of chemical mechanical polishing (CMP) and the metal film deposition that cause conventional characters to have limited readability is minimized.

The small size of the marks in the range of 1 to 13 μm , as set forth in the present claims, permits locating the marks on an inner surface of a V-shaped notch of the wafer, also as set forth in applicant's claims. Due to the size and location of the marks, as presently claimed, the influences of wafer processing, such as chemical mechanical polishing and chemical film deposition, which adversely affect the conventional IDs, can be minimized. This means that after wafer processing the markings in accordance with applicant's claimed invention can be easily read, whereas those of the conventional IDs cannot be read. The teachings of Iwai, Jeng, Yano and/or Oishi do not remotely contemplate or suggest the size of the dot markings or the arrangement thereon as required in applicant's claimed invention. Therefore, applicant respectfully submits that the presently claimed invention is distinguishable from these teachings.

For example, the teachings of Iwai are directed to alignment marks, and desire to make the alignment marks as large as possible. These teachings do not remotely contemplate or suggest an identification system using dot marks of a maximum length of 1 to 13 μm that are arranged at a specific location within a notch on an outer peripheral face of the semiconductor wafer, as required in the present claims. Applicant respectfully submits that it would have been impossible for a person skilled in the art to be motivated to the presently claimed invention from the teachings of Iwai.

The teachings of Jeng are also directed to alignment and monitor marks, and not identification marks. Applicant respectfully submits that such monitor marks are not relevant to the presently claimed invention. Further, since Jeng proposes marking the surface of a wafer, such markings would be destroyed when conducting the processing of the wafer, such as chemical mechanical polishing and methyl film deposition. For the same reasons as set forth above with respect to the teachings of the Iwai, applicant respectfully submits that it would have been impossible for a person skilled in the art to be motivated to the presently claimed invention from the teachings of Jeng.

The teachings of Yano propose marking the side surface of a semiconductor wafer. These teachings teach away from the presently claimed invention by describing that it is preferable to provide the identification propose therein at a place on the semiconductor wafer other than the notch. This is directly opposite to the presently claimed invention. See, for example, Yano at column 8, line 26-36. Since Yano proposes marking the side of the wafer, the teachings of Yano encompass markings of relatively large size. For all these reasons, applicant respectfully submits that the teachings of Yano would not motivate one of ordinary skill in the art to provide marks on semiconductor wafers of a maximum size of 13 microns, where such marks are provided within the notches on the peripheral surface of the semiconductor wafer, as presently claimed, so that abrasion from conventional semiconductor wafer treatments can be avoided.

Teachings of Oishi propose a wafer without a notch. Thus, it is impossible for such teachings to motivate one of ordinary skill in the art to provide markings within the notch, as required in the present claims. In summary, neither the teachings of Oishi nor Yano provide any motivation or suggestion to one of ordinary skill in the art for providing markings of a size as required by the present claims at the location, as required by the present claims, which includes locating the dot not within a notch on a peripheral surface of the semiconductor wafer.

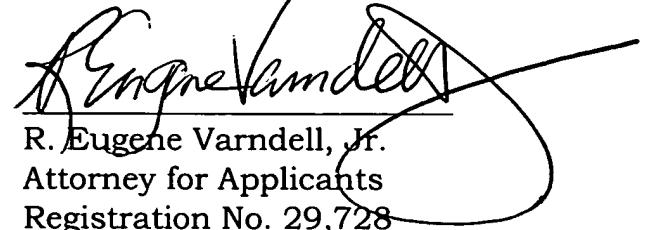
For the foregoing reasons, applicant respectfully submits that none of the teachings of Iwai, Jeng, Yano and Oishi, either taken alone or in combination, contemplate or suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103. Therefore, applicant respectfully requests that the examiner reconsider and withdraw all the prior art rejections of applicant's claims in the outstanding Office action.

In view of the foregoing amendments and remarks, favorable consideration and allowance of claims 1-9 are respectfully requested. While it is believed that all the claims in this application are in condition for allowance, should the examiner have any comments or questions, it is respectfully requested that the undersigned be telephoned at the below-listed number to resolve any outstanding issues.

In the event that this paper is not timely filed, applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized

to charge the fee therefor, as well as any deficiency in the payment of the required fee(s) or credit any overpayment, to our Deposit Account No. 22-0256.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at page 23, line 15, has been amended as follows:

-- A plane shape of the notch 1 is as shown by Fig. 2. In plane view, a longest dimension from a side face of the wafer W to a bottom portion of the notch 1 falls in a range of 1 to 1.25 mm, the bottom portion defines a circular arc face, a radius of curvature thereof is determined to be equal to or larger than 0.9 mm and an angle of an opening extended linearly from the bottom portion and opened at the side face of the wafer is 90 degree. Further, also an end edge of the opening is chamfered by [R] 0.9 mm and accordingly, a linear portion except the circular arc face portion of the bottom portion of the notch 1 becomes 0.669 mm at maximum. --

IN THE CLAIMS:

Claim 9 was amended as follows:

-- 9. The semiconductor wafer according to Claim 1, wherein the [a] dot mark has a height in the range of 0.005 to 5 μm . --